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PCB Layout

PCB Layout: Regulatory requirements

- Safety Agencies will control:
  - The PCB material used
  - Creepage distances – shortest path between two parts along the SURFACE
    - Grooves don’t count if less than a certain width
  - Clearance distances – shortest path between two parts through air
    - PCB slots can be used to increase creepage – but not always clearance
- Safety, EN 62368-1 (replaces EN60950 – Date Of Withdrawal - 2019)

PCB Layout – Grounding and Ground Planes

- Ideal Ground Plane is an Infinite Equipotential Surface
- Practical Ground Plane is a bounded ‘almost Equipotential’ Surface
- Return current in ground plane will follow the path of the outward bound conductor
  - ‘Image Current’ – minimises loop area and inductance, maximises capacitance and minimises impedance
- Do’s and Don’t’s
  - Don’t put slots in the ground plane
- Ground planes are not possible on a single sided board (SSB)
  - Take extra care to minimise the impedance in the ground connections in a SSB
  - Low impedance from AGND to PGND is desirable
  - Place as much grounded copper under the IC as possible
  - Remember that DC tracks are an AC Ground

UCC28600

8-pin Quasi-Resonant Green Mode PWM Controller

Efficiency Requirements

- Energy Star®
  - Single voltage external AC-DC and AC-AC power supplies
  - Power supplied to be labeled with efficiency grade
  - Active mode efficiency based upon calculation of the simple average of 25%, 50%, 75%, and 100% of full rated power at nominal input

Rated Output Power (P_{OUT})	Minimum Efficiency (η)
$0W \le P_{OUT} \le 1W$	$\eta \ge 0.48 \times P_{OUT} + 0.14$
	$\eta \ge 0.497 \times P_{OUT} + 0.067$
$1W < P_{OUT} \le 49W$	$\eta \ge [0.0626 \times \ln(P_{OUT})] + 0.622$
	$\eta \ge [0.0750 \times \ln(P_{OUT})] + 0.561$
$49W < P_{OUT} \le 250W$	$\eta \ge 0.87$
	$\eta \ge 0.86$
$P_{IN} = 100W$	PF $\ge$ 0.9 @ 100% load
	$V_{OUT} < 6V$, $I_{OUT} \ge 0.55A$

  - No-Load (Stand By) mode measured with open output

Rated Output Power (P_{OUT})	Maximum Input Power (P_{IN})
$0W \le P_{OUT} < 50W$	$P_{IN} \le 0.3W$
	(0.5W for AC/AC)
$50W \le P_{OUT} \le 250W$	$P_{IN} \le 0.5W$

UCC28600: Features

- 8 Pin Quasi-Resonant Flyback Green Mode Controller
- Current Mode Controller
- Quasi-Resonant Mode For Reduced EMI And Low Switching Losses (Valley Switching)
- Low Stand By Current For Low System No-load Power Consumption
- Protection Features:
  - Programmable Line Over Voltage Protection
  - Programmable Load Over Voltage Protection
  - Internal Over Temperature Protection
  - Cycle By Cycle Power Limit
  - Over Current Hiccup Restart Mode
- Green Mode STATUS Pin To Disable PFC During Light Load
- 1A Sink/0.75A Source TrueDrive™ Gate Drive Output
- Multi-mode Operation For Energy Efficiency Over Entire Range Of Operation

UCC28600

- Simplified Application

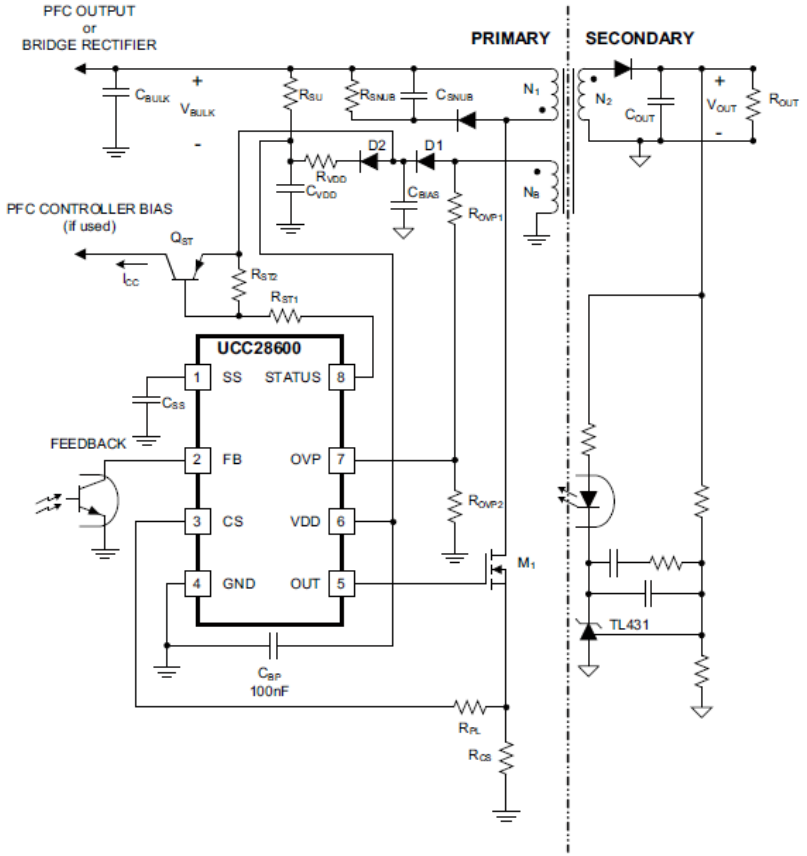


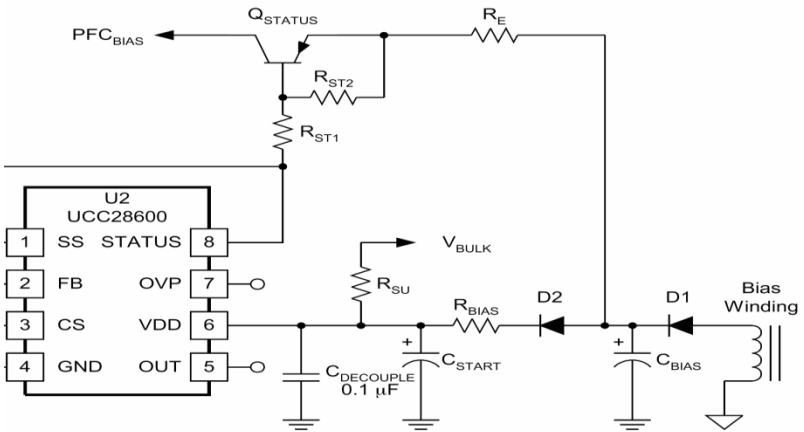
Figure 13. Simplified Application

UCC28600: VDD

- Low start up current (12μA typical) enables use of high value start up resistors from rectified input bus (R_{SU} = 2+ MΩ)
  - PFC stage will be off at start up
- Operating energy supplied by auxiliary bias winding
  - Light load conditions, bias winding voltage will be lower than full load conditions
- C_{BIAS} must be large enough to hold up

  VDD during burst packet period
- Use a 0.1μF ceramic capacitor to GND

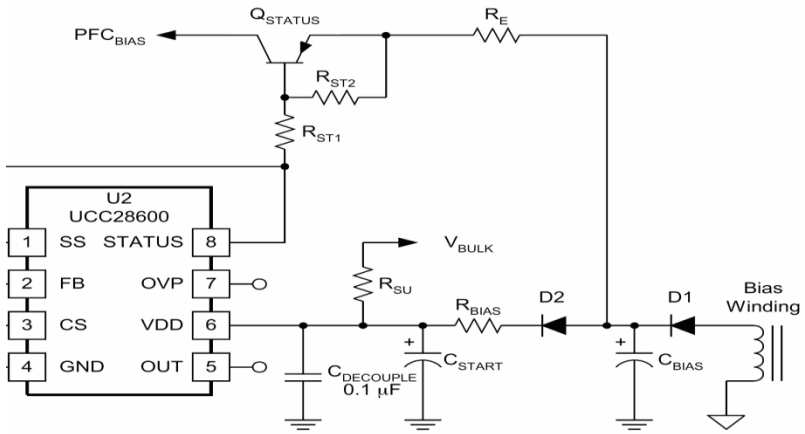
  pin for high frequency filtering



UCC28600: VDD (cont.)

- Additional C_{START}/D_2 required to isolate STATUS from start up resistors (R_{SU})
  - When VDD < UVLO internal floating
    gates divert startup current from VDD
- Series resistor with bias winding to limit transients from leakage inductance and drain capacitance
  - Needed To Prevent OVP Triggering During Transients

$$R_{BIAS} = \frac{\pi}{4} \cdot \frac{N_B}{N_P} \cdot \left[\frac{V_{DSovershoot} \cdot f_{max} \cdot \sqrt{L_{leak} \cdot (C_{DRAIN} + C_{SNUB})}}{I_{DD} + C_{ISS} \cdot V_{GATE} f_{max}} \right]$$



UCC28600: SS

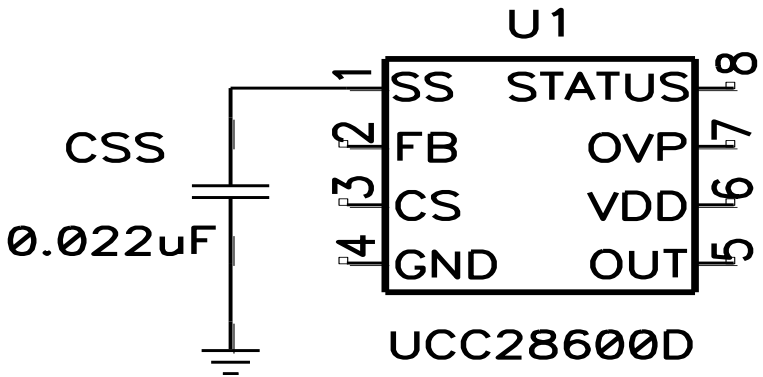
- All faults discharge SS to GND (except PL)
- C_{SS} must be chosen so as to not trigger power limit when charging output caps
- Layout is important

$$C_{SS} > I_{SSchg} \cdot \frac{\left(\frac{-R_{OUT} \cdot C_{OUT}}{2}\right) \cdot \ln\left[1 - \frac{\left(V_{OUT} - \Delta V_{OUTstep}\right)^2}{R_{OUT} \cdot P_{LIMIT}}\right]}{A_{CS\_FB}\left(V_{PL} - V_{CSoffset}\right)}$$

$$V_{PL} := 1.2V$$

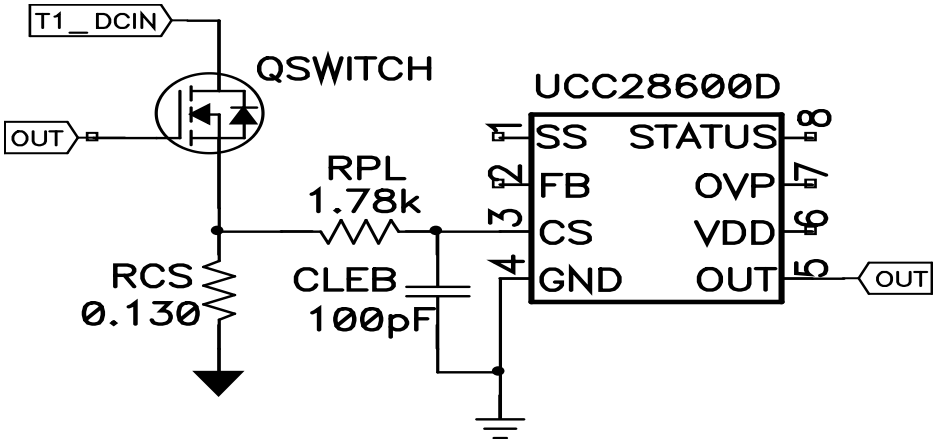
$$V_{CSoffset} := 0.4V$$

$$A_{CS\_FB} := 2.5$$



UCC28600: CS

- Power Limit
  - Triggered at V_{CS} = 0.8V
  - Design Calculator uses "Pout, max limit" as Power Limit set point
    - Line dependent
  - Uses current sourced by OVP to add an offset proportional to line voltage
    - DCM converter but CS has ramp-on-a-step waveform due to power limit offset
  - Will not trigger SS discharge
- Over current shutdown
  - Triggered when V_{CS} = 1.25V
- R_{PL} and capacitor to GND for noise filter



UCC28600: OVP

- Provides information proportional to the drain voltage
  - Valley Detection
  - Line over-voltage
    - Note: spec has very wide range
  - Load over-voltage
  - Provides internal I_{LINE} current
- Crucial to have bias windings well coupled to both primary and secondary

$$R_{OVP1} = \frac{\frac{N_B}{N_P} \cdot V_{BULKshutdown}}{450 \cdot \mu A}$$

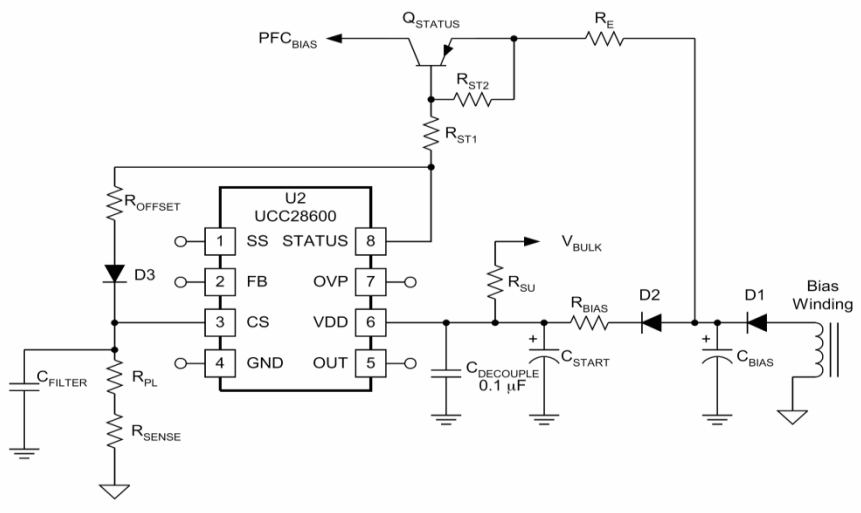
$$R_{OVP2} = \frac{R_{OVP1}}{\left(\frac{N_B}{N_S} \cdot \frac{V_{OUTshutdown} + V_F}{3.75V} \right) - 1}$$

UCC28600: OVP (cont.)

OVP				
EVENT	EVENT CONDITIONS		RESULT	
LINE OVER VOLTAGE	OUT = HIGH; OVP IS PROPORTIONAL TO LINE VOLTAGE	IF OVP CLAMPED TO 0V AND SOURCING 450uA LINE OVER VOLTAGE IS DETECTED	- TURNS OFF OUTPUT - AUX WINDING FALLS - VDD FALLS BELOW UVLO - SS DISCHARGES - TURN ON WHEN SS RE-CHARGES	CHECKED EVERY CYCLE
OUTPUT OVER VOLTAGE	OUT = LOW; OVP IS PROPORTIONAL TO OUTPUT VOLTAGE	IF OVP = 3.75V OUTPUT OVER VOLTAGE IS DETECTED	- TURNS OFF OUTPUT - AUX WINDING FALLS - VDD FALLS BELOW UVLO - SS DISCHARGES - TURN ON WHEN SS RE-CHARGES	CHECKED EVERY CYCLE
VALLEY DETECT	OUT = LOW	OVP DETECTS DEMAGNETIZED CORE FROM 0V TRANSITION	- QR TAKES PRECEDENCE - OUTPUT TURNED ON IF RUNNING < 130kHz - AT 130kHz, TURN ON AT NEXT VALLEY THAT WOULD RESULT IN fs < 130kHz - TURN-OFF BY PEAK CURRENT PWM CONTROL	CHECKED EVERY CYCLE

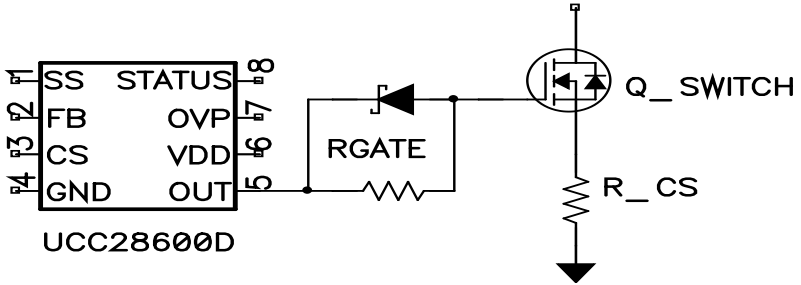
UCC28600: STATUS

- Active High: drives base of PNP to provide bias to PFC controller
- High during UVLO and SS
  - PFC stage off
- Select R_{ST1} and R_{ST2} to operate Q_{STATUS} in saturation/cutoff
- Careful selection of R_{ST1} and R_{ST2} so Q_{STATUS} doesn't turn on during green-mode
- Can be used to eliminate audible noise



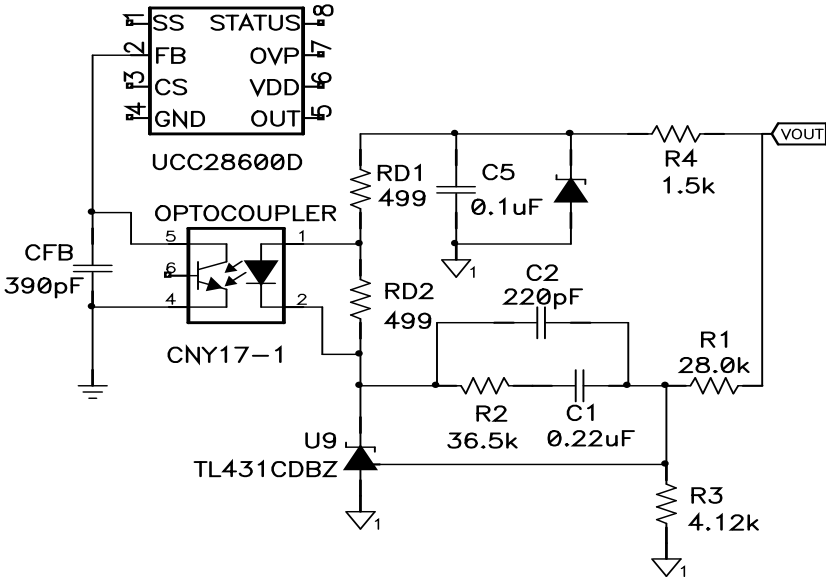
UCC28600: OUT

- Internally Clamped To 13V Or VDD Whichever Is Lower
- TrueDrive Provides 1A+ Of Current Sink Where It Counts, During MOSFET Turn Off
  - Use parallel diode to speed up turn off



UCC28600: FB

- Collector of Opto tied directly to FB
- FB has internal 20kΩ pull-up resistor to the 5V reference
- Maximum duty cycle is when FB is high and zero duty cycle is when FB is low.
- Capacitor on FB provides delay time for over load protection: **390pF max value**
- FB internal thresholds play a key role in determining operating mode



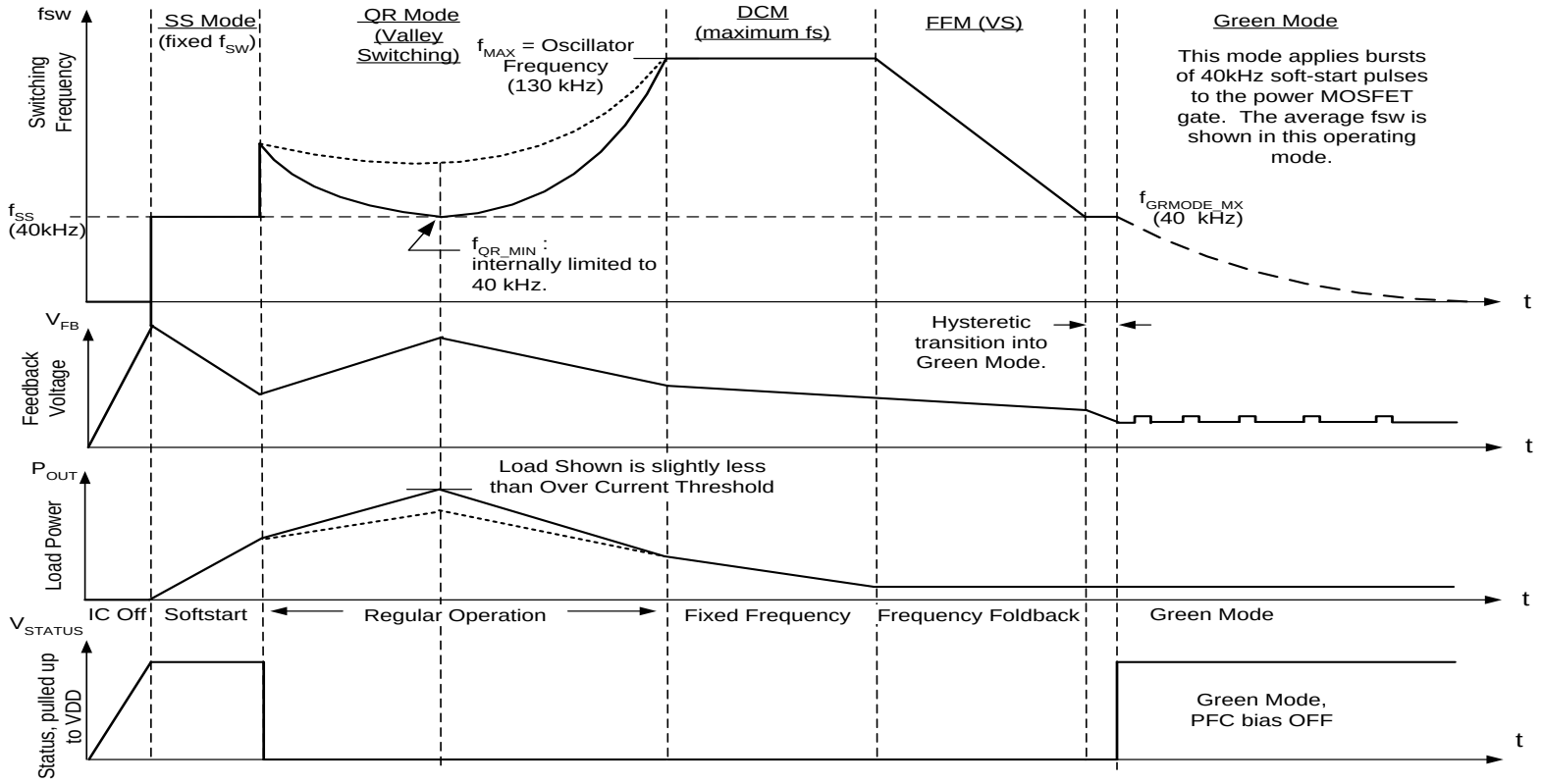
UCC28600: MODES

- V_{FB} Thresholds Determine Operating Mode
- Mode Depends Upon Boundaries Set By
  - Magnetizing inductance
  - Reflected output voltage
  - Input Voltage Range
- Minor manipulations can be made by V_{CS} through iterative selection of
  - R_{CS}
  - R_{PL}
  - R_{OVP1}
  - R_{OVP2}

UCC28600: MODES (cont.)

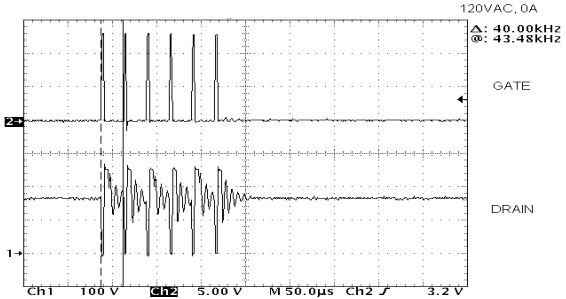
- UCC28600 always operates in current mode control
- FB controls operating mode
  - 30% ≤ I_{LOAD} ≤ 100% : QR or DCM
    - 2V ≤ FB ≤ 4V
    - Clamped f_{MAX}
    - Valley switching
    - 0.4V ≤ CS ≤ 0.8V
  - 10% ≤ I_{LOAD} ≤ 30% : FFM
    - 1.4V ≤ FB ≤ 2V
    - 40kHz ≤ f_{MAX} ≤ 130kHz
    - Valley switching
    - CS = 0.4V
  - 0% ≤ I_{LOAD} ≤ 10% : Burst
    - 0.5V ≤ FB ≤ 1.4V
    - Switching within burst packets is 40kHz
    - CS < 0.4V

UCC28600: MODES (cont.)

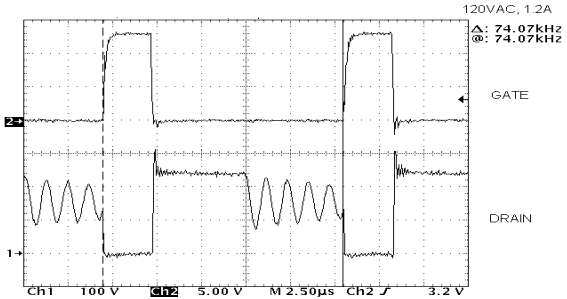


UCC28600: MODES (cont.)

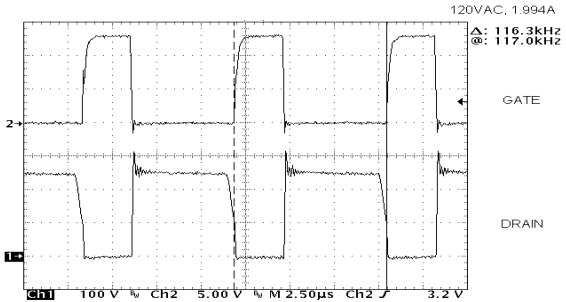
GREEN MODE
120VAC IN, 0.0A



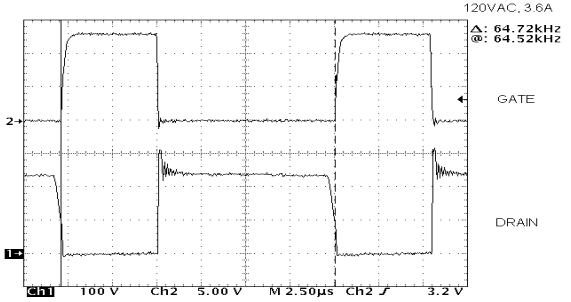
FFM
120VAC IN, 1.2A



Critical Conduction
120VAC IN, 1.99A



QR MODE
120VAC IN, 3.6A



Consider Layout Before the Board is Built

- Minimize the high current loops to reduce parasitic capacitances and inductances.
  - But do not make traces with a high dv/dt too wide as this will create a very good E-field antenna.
- Separate the IC signal ground from the high current power ground in order to isolate the noise away from the IC substrate. The separate grounds should be tied together at the input capacitor on the primary side.
- Returning the sense resistor to the input capacitor, instead of to the ground plane under the IC, is also required for a successful design.
- The decoupling capacitor on VDD must be placed as close as possible to the VDD and GND pins of the IC.
- The FB trace should be short and as far away from noise as possible.
- Use a short, wide trace width for the gate drive
- Use a small value gate drive resistor in series with the gate drive to control the turn on transition time and reduce the dv/dt ringing in this node.
- A 10k resistor is placed between the gate of the MOSFET and ground to discharge the gate capacitance and protect against inadvertent dv/dt triggered turn-on.
- Adding a small capacitor, C_{FILTER}, to the CS pin will create an RC low pass filter in conjunction with the power limit resistor, R_{PL}, and will improve noise immunity at the current sense pin.

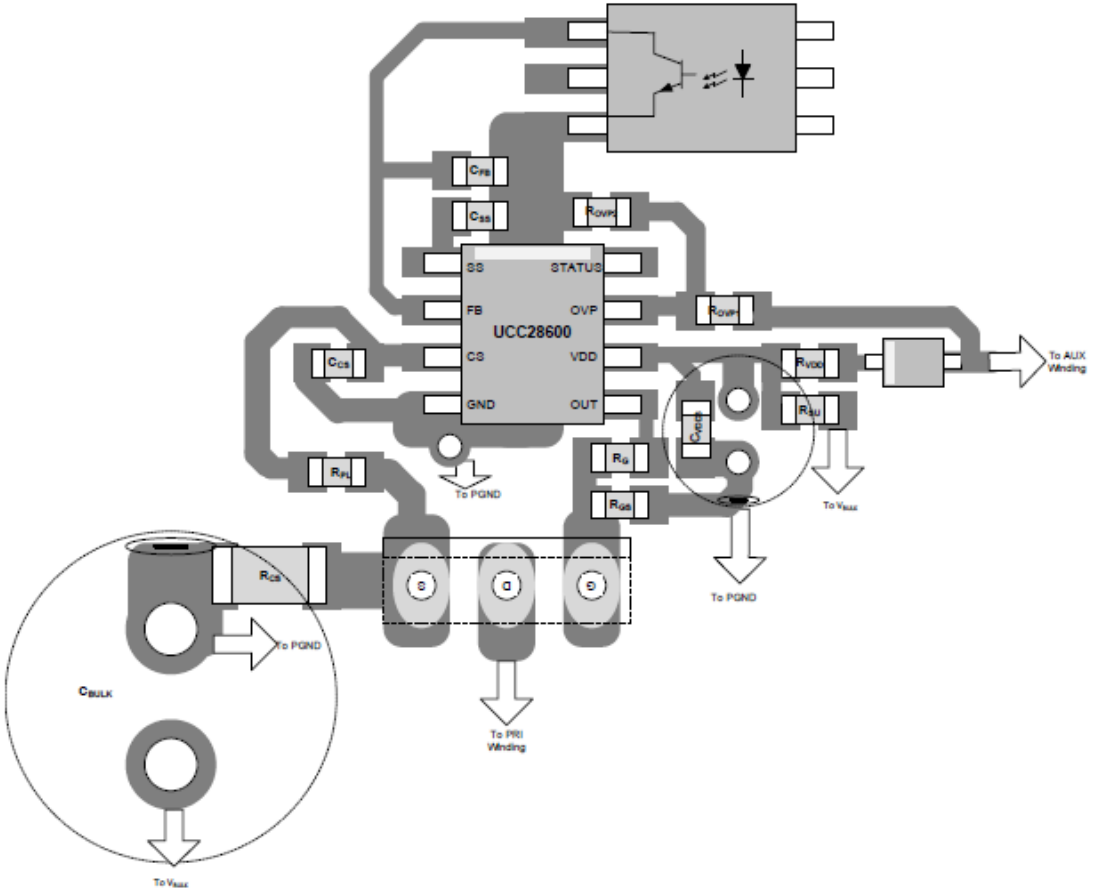


Figure 25. Partial Layout Example Showing Component Placement